

AMENDMENT UNDER 37 C.F.R. § 1.111
U.S. Application No.: 10/758,040
Attorney Docket No.: Q78894

REMARKS

Reconsideration and allowance of the subject application are respectfully requested. Claims 1-10 are all the claims pending in the application. Applicant respectfully submits that the pending claims define patentable subject matter.

Priority

Applicant submits herewith a certified copy of the foreign priority documents, and respectfully asks that the Examiner acknowledge receipt of the same in the next communication.

Claim Objections

Claim 1 stands objected to by the Examiner because claim 1 recites the subject matter “the first memory” in line 12 instead of --a first memory--. Applicant has amended claim 1 to recite --a first memory--, and accordingly, the objection to claim 1 should be withdrawn.

Claim Rejections - 35 U.S.C. § 101

Claim 10 stands rejected under 35 U.S.C. § 101 because the claimed invention is allegedly directed to non-statutory subject matter.

The Examiner maintains that claim 10 is not limited to tangible embodiments. In particular, the Examiner states that in view of the Applicant’s disclosure, specification page 48, paragraph [133], the medium is not limited to tangible embodiments, instead being defined as including both tangible embodiments (e.g., recordable type media such as ROM, floppy disks and hard disks, CD-ROMs, DVDs, etc.) and intangible embodiments (e.g., transmission type media such as carrier waves).

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Although Applicant believes that claim 10 is directed to tangible embodiments, Applicant herein amends claim 10 to address the Examiner's rejection. Accordingly, the 35 U.S.C. § 101 rejection of claim 10 should be withdrawn.

Claim Rejections - 35 U.S.C. § 103

A. Claim 1

Claim 1 stands rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Bourke et al. [US 5,509,124 A; hereinafter Bourke] in view of Barrenscheen et al. [US 2003/0084226 A1; Barrenscheen]. Applicant respectfully traverses the 35 U.S.C. § 103 rejection, as set forth below.

The Examiner concedes that "Bourke does not teach that the multiplexer receives first data from the processor and transfers the received first data to a first memory through a synchronous data bus synchronized with the processor, or receives second data from the first memory through the synchronous data bus and transfers the received second data to the processor." (Office Action, page 4)

The Examiner alleges that Barrenscheen discloses the missing features. Particularly, the Examiner asserts that bus interface BI1 in Fig. 4 is a multiplexer that operates in the manner disclosed in claim 1.

However, bus interface BI1 is not a multiplexer. Instead, bus interfaces BI1-BI4 are used to connect the data transmission device DTU to the first through fourth buses BUS1-BUS4, respectively. Consequently, bus interface BI1 does not perform the functions of and is not described as a multiplexer in Barrenscheen.

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Further, the Examiner maintains that BUS1 in Figs. 2A-B is synchronized with the processor. Barrenscheen, however, does not indicate in paragraph [0035], lines 11-12 or Figs. 2A-B that BUS1 or BUS2 is synchronized with the processor. Although the DTU used as a DMA in paragraph [0035] can transfer data between BUS1 and BUS2, and between their respective devices, Barrenscheen does not require BUS1 or BUS2 to be synchronized with the processor in Figs. 2A-B or paragraph [0035]. Barrenscheen is silent with respect to this feature.

For at least the foregoing reasons, claim 1 is not anticipated or rendered obvious by the individual or combined teachings of Bourke and Barrenscheen. Therefore, the 35 U.S.C. § 103 rejection of claim 1 should be withdrawn.

B. Independent claims 2, 4, and 10

Claims 2-6 stand rejected under 35 U S C 103(a) as allegedly being unpatentable over Masayuki et al. [JP 2000-92365 A; cited by the Applicant; hereinafter Masayuki] in view of Barrenscheen [US 2003/0084226 A1].

Claim 7-9 stand rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Masayuki [JP 2000-92365 A] In view of Barrenscheen [US 2003/0084226 A1] as applied to claims 2-6 above and further in view of Sodos [US 5,239,651 A].

Claim 10 stands rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Masayuki [JP 2000-92365 A] in view of Barrenscheen [US 2003/0084226 A1] and what was well known in the art, as exemplified by Luo et al. [US 6,265,885 B1; hereinafter Luo].

Applicant respectfully traverses the 35 U.S.C. § 103 rejections, as set forth below.

Applicant submits that Masayuki (*the primary reference*) fails to teach or suggest **both** a synchronous data bus synchronized with a processor and an asynchronous data bus not synchronized with the processor, which is required in claims 2, 4, and 10.

It appears the Examiner believes that CPU bus 34 is (synchronous) synchronized with CPU 41, and he may assume that image data bus 33 is (asynchronous) not synchronized with CPU 41 because image data bus 33 is not directly connected to CPU 41 in Fig. 2. However, paragraph [0028] of Masayuki makes no disclosure that image data bus 33 is asynchronous. Moreover, Masayuki does not disclose any terms related to “synchronous” and “asynchronous”.

Further, Applicant submits that it is not inherent that image data bus 33 is (asynchronous) not synchronized with CPU 41 in Fig. 2, because evidence of inherency in a reference “must make it clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill.” Continental Can Co. USA Inc. v. Monsanto Co., 948 F.2d 1264, 1269 (Fed. Cir. 1991) (emphasis added). Additionally, “Inherency, however may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient.” Id. Even if the prior art reference could have equally been used or made with only two possibilities, a patent claim which claims one of the two possibilities will not be anticipated because that limitation was not “necessarily” present in the prior art disclosure. See Finnigan Corp. v. I.T.C., 51 U.S.P.Q.2d 1001, 1009-10 (Fed. Cir. 1999) (holding that a prior art reference that disclosed a set-up for performing only resonance or nonresonance ejection was insufficient to show, clearly and convincingly, that nonresonance ejection was inherently taught by the prior art reference).

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Similarly, even if the image data bus 33 could either be synchronized or not synchronized with CPU 41, this possibility cannot be said to disclose that the image data bus is *necessarily* not synchronized when Masayuki is silent with respect to this feature.

As discussed above, Barrenscheen does not disclose whether or not BUS1 or BUS2 is synchronous. Sodos and Luo do not compensate for the deficiencies of Barrenscheen and Masayuki to meet the particular requirements of independent claims 2, 4, and 10.

Even taken as a whole for what they would have meant to a skilled artisan, the individual or combined teachings of Masayuki, Barrenscheen, Sodos and Luo do not anticipate or render obvious the features of independent claims 2, 4, and 10.

For at least the foregoing reasons, claims 2, 4, and 10 are patentable over the applied art. Therefore, the 35 U.S.C. § 103 rejection of claims 2-10 should be withdrawn.

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

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Respectfully submitted,



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